NC STATE UNIVERSITY

ECE 792-036 : Advanced Verification with UVM
Fall 2018
Course Overview

Instructor: Robert D. Oden
Office Hours: Announced weekly
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Textbook:
"Universal Verification Methodology Class Reference Manual" (Accelera), 2013. Available online.

Prerequisite: ECE 745 ASIC Verification or equivalent.

Course Objectives

1. To prepare the student to be a staff-level ASIC or FPGA verification engineer.
2. To give the student the ability to architect and implement simulation environments using UVM.
3. To give the student an understanding of the issues related to verification reuse and emulation, with a focus on the Universal Verification Methodology base class library.

Course Outcomes

1. Students will be able to verify complex digital designs at block and chip level, identifying the contained bugs, and closing functional coverage, using UVM.
2. Students will demonstrate an understanding of advanced verification methodologies and industry best practices used in ASIC Verification and their implementation using UVM.

Course Approach:

The course approach is similar to how the instructor teaches UVM to engineering professionals. All instructional material will be delivered during lectures. Lecture materials will include conceptual descriptions, examples, and sample code. Questions during lectures is recommended and encouraged. Instructional flow reflects typical verification development flow for production designs.

The course contains three projects. The projects build upon each other. The content created in the first project will be used in the second project. The content created in the second project will be used in the third project. There will be a test prior to the first and second project to ensure readiness for project development. Students will have aproximately four weeks to complete each project. The first two projects will be done individually. The third project will be done in groups of five students. Projects developed will reflect architectures and techniques typically used for ASIC and FPGA verification of production designs.

The course contains three tests. The first test will be held in week 4 or soon thereafter. The second test will be held in week 8 or soon thereafter. Test questions reflect typical interview questions on UVM. Therefore, tests are closed book and closed-notes.

The audit requirement is to complete the first project and tests to a B standard or better.

Student Evaluation

Item	Contribution
Test 1	10%
Project 1	20%
Test 2	10%
Project 2	25%
Project 3	25%
Final Test	10%