ECE 792-046
Quantum Computer Architecture

Instructor(s): Prof. Eric Rotenberg (ericro@ncsu.edu)

Objective or Description: Understand and practice quantum computing from a computer architecture perspective. The focus is quantum computer architecture: quantum bits and logic gates, quantum microarchitecture, and quantum instruction-set architecture.

Prerequisites: ECE 563 (Microprocessor Architecture)

Textbook:

Quantum Computing for Computer Architects, 2nd edition, Tzvetan S. Metodi, Arvin I. Faruque, Frederic T. Chong.

View a free on-line PDF copy:

https://www.morganclaypool.com/doi/pdf/10.2200/S00331ED1V01Y201101CAC013

Topics:

Context:
Large mainstream hardware/software companies have already begun significant investments in building quantum computers and retooling abstractions like dev kits, programming languages, compilers, computer architecture (ISA and microarchitecture), and gates. Microsoft is helping traditional hardware/software folks reason about expressing problems for quantum computing: see this interesting article.

Topics:
- Expressing a problem for quantum computing: what is the input and output of a quantum computation and how does one make sense of it?
- Quantum logic gates (*e.g.*, CNOT, Hadamard, Toffoli) and other quantum operations (*e.g.*, teleportation)
- Quantum instruction set architectures (ISA)
- Quantum microarchitectures

Topics for each lecture period will be drawn from the textbook and also research papers from the ISCA/MICRO community. Topics will be assigned to each pair of students, and each pair of students and the instructor will take turns reading about their topic, assimilating the topic, and presenting a lecture on that topic using a powerpoint template and lecture guidelines. There may be a brief quiz at the beginning of each lecture (composed by the presenters and/or instructor), followed by classroom Q&A/discussion of the quiz, followed by the formal lecture to clean up the ideas.

superposition, where each state holds the result of the addition. Quantum adders are integral to the circuit for quantum modular exponentiation used in Shor's quantum factoring algorithm.

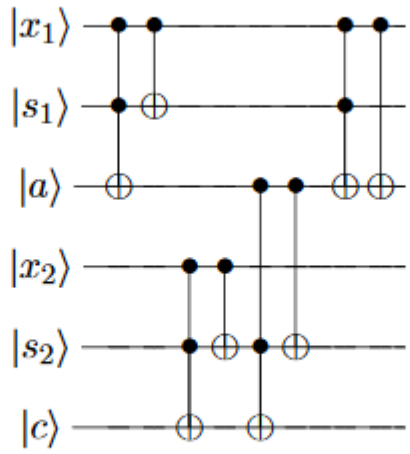

Figure 2.5: Two-Bit Adder composed of quantum controlled-NOT (CNOT) and Toffoli gates. The circuit adds the two bitstrings "(x_1, x_2)" and "(s_1, s_2)", where the least significant bit is the leftmost bit. The result is stored in the bitstring "(s_1, s_2, C), where C is the carry-out bit.

Grading:

- Lecture and quiz preparation (prepared by pairs of students): 20%
- Quizzes (taken by all students): 10%
- Midterm exam: 20%
- Research project: 50% [Note: infrastructure, simulator, *etc*., for projects is not yet defined]

The intensity of this course will be no more than ECE 563.

Cross-listing in other departments: none